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for

METHOD AND APPARATUS FOR ADJUSTING AN ACTIVE FILTER

Method and Apparatus for Adjusting an Active Filter

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application is a continuation of the Patent Cooperation Treaty application PCT/EP02/04528, having an international filing date of April 24, 2003, which application is hereby incorporated by reference in its entirety, and to which priority is claimed, and which claims priority to German Application Serial No. DE 101 21 517.7, filed on May 3, 2001.

BACKGROUND OF THE INVENTION

1. The Field of the Invention

[002] The present invention relates to a method and a circuit arrangement for adjusting an active filter in determining frequency response.

2. The Relevant Technology

[003] Active filters are used, for example, in telecommunication networks. In this case, active filters are used, particularly for digital transmission methods, as input and output filters upstream of an analogue-digital converter and downstream of a digital-analogue converter, respectively. In a digital technology application, it is important for a particular nominal frequency response to be observed on the basis of the clock frequencies used in the digital system. If the elements used in an active filter to determine frequency response are capacitors, inter alia, which disadvantageously vary greatly in production, it is generally necessary to have a means of alignment for setting the frequency response. Normally, such active filters

for use in telecommunication networks are integrated in a semiconductor together with an alignment circuit.

[004] By way of example, VDSL systems require an active low-pass filter whose cut-off frequency needs to be able to be set to one of a plurality of frequencies between 8 and 12.44 MHz, the permissible tolerance being ± 5% of the frequency value. If a set of capacitors which determine frequency response is now used for each adjustable nominal frequency together with the respective alignment circuit required, the result is disadvantageously a very high level of circuit complexity, whose scope entails further drawbacks, such as parasitic capacitances.

BRIEF SUMMARY OF THE INVENTION

[005] The present invention provides a circuit arrangement and a method for adjusting an active filter of the type mentioned initially which allow one frequency response from a plurality to be set with a high level of accuracy given little circuit complexity.

[006] The inventive method involves the use of a memory arrangement which contains parameters for varying the adjustable capacitor to determine frequency response. The selection of the parameters takes into account the intended nominal cut-off frequency or the nominal frequency response and a measure of the actual frequency response of the active filter. The adjustment is advantageously possible in one work step, so that it is not necessary to first set the nominal frequency response and then to align it in a further step.

[007] Advantageously, the measure of the frequency response of the filter is ascertained using a reference capacitor whose value is in a known ratio to the value of the filter's capacitors which determine frequency response. In this case, a measure of the value of the reference capacitor can be ascertained. This value can be used to infer the value of the capacitor in the filter or to infer the frequency response of the filter. This means that it is not necessary for the filter to have a circuit for determining the measure of the frequency response connected to it which might impair the operation of the filter, for example, as a result of parasitic capacitances or contact resistances of added switches.

[008] The use of a reference capacitor is particularly appropriate when at least all of the capacitors are integrated on a chip or semiconductor. In which case, the absolute values of the

capacitors can vary but the ratio of the values of the various capacitors to one another is easily reproducible and accurately determinable or is known. Thus, provision can be made, in particular, for all the capacitors to be formed from standard capacitors of the same value by connecting at least one standard capacitor in parallel or in series. In particular, the ratio of the reference capacitor to another capacitor is determined by the number and type of the combination of the respective interconnected standard capacitors.

[009] Advantageously, a time constant is determined as a measure of the frequency response. This time constant is able to be ascertained particularly easily by means of time measurement. Therefore, by way of example, a step signal can be connected to the input of the filter or to the reference capacitor. In addition, a measurement may be obtained from the time taken until the output signal from the filter or a voltage across the reference capacitor reaches a particular value.

[010] Normalizing the time constant to a particular measurement frequency allows the actual frequency response to be measured at any frequencies regardless of the nominal cut-off frequency.

[011] If the memory arrangement used is an addressable table memory, then it is a particularly simple matter to select the adjustment parameters for the adjustable capacitor. The adjustment parameters are selected by splitting a multidigit address range in the table memory and addressing another part using the selection of the nominal cut-off frequency and addressing the other part using the measure of the actual frequency response. By way of

example, in an address range comprising 10 bits, 3 bits can be used to select a particular nominal filter frequency, where a total of eight nominal filter frequencies would be selectable. The remaining 7 bits can be used to input the measure of the actual frequency response.

[012] In this case, the adjustment parameters stored in the memory arrangement allow the capacitor to determine the frequency response to be adjusted with sufficient accuracy. The accurate adjustment makes the desired nominal frequency response and the alignment possible.

[013] Advantageously, the adjustable capacitor has a plurality of series circuits connected in parallel with each including a single capacitor and a switch. The total capacitance of this circuit arrangement is obtained from the sum of the single capacitors connected in series with closed switches. In this context, provision can be made for the values of the single capacitors to behave as integer powers of two towards one another. Thus, a binary word stored as an adjustment parameter can advantageously be used directly for closing the switches or for adjusting the capacitor. The adjustable capacitor can also have a base capacitor which has a circuit arrangement of variable capacitance connected in parallel with it, which means that the adjustment range for the adjustable capacitor can be smaller.

[014] For adjusting the capacitor, provision can be made for the measurement of the actual frequency response and the subsequent selection of an adjustment parameter to be carried out a plurality of times in order to achieve a higher level of accuracy. Particularly, the measurements are useful in those cases in which the effect of an adjustment action for the

adjustable capacitor cannot be determined in advance. This can be the case, by way of example, in parallel-connected and individually connectable single capacitors, on account of manufacturing tolerances in the single capacitors. Should the connected single capacitor have a different value from the one taken as a basis for the adjustment parameter in such a case, then the difference can be ascertained in a second measurement and the adjustment can be repeated.

[015] If the active filter is integrated in a semiconductor together with all of the components required for carrying out the inventive method, then the costs therefor can be reduced. Particularly, the cost is further reduced if the inventive circuit arrangement is required in very large quantities, for example, when used in a telecommunication network.

[016] These and other objectives and features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[017] To further clarify the above and other advantages and features of the present invention, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[018] Figure 1 illustrates the design of an active filter with the components which determine frequency response, and

[019] Figure 2 is a block diagram illustrating the active filter together with the components required for adjustment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[020] Figure 1 shows a third-order Chebyshev low-pass filter. In this regard, the filter 1 has an operational amplifier 5 and, for the purpose of external connection, resistors 4 and capacitors 2, 3 which determine the frequency response of the filter 1. The capacitors 2 are each fixed capacitors, whereas the capacitors 3 are adjustable.

[021] The adjustable capacitors 3 each comprise a parallel circuit comprising single capacitors 6 which are connected in series with switches 7. The single capacitors 6 in an adjustable capacitor have different values which behave like integer powers of two towards one another.

[022] The value of the base capacitor 2 is proportioned such that, when the adjustable capacitor 3 is adjusted to the smallest possible value, i.e. when all the switches 7 are opened, a cut-off frequency for the filter 1 is achieved which, taking into account usual manufacturing tolerances, is above the highest cut-off frequency which can be set.

[023] The filter 1 shown in Figure 1 is provided for use in a VDSL system and is intended to be used there as an input or output filter upstream of an analogue-digital converter or downstream of a digital-analogue converter.

[024] Figure 2 shows a block diagram of the active filter 1 together with the components which are required for carrying out the method. The components are divided into an analogue part A and a digital part B. The analogue part A has the active filter 1 together with a device 8

for determining a measure of the frequency response of the filter 1. The digital part B has a control device 9 and a memory device 10. The control device 9 receives a clock signal via a clock input 13. In addition, the control device 9 is connected by means of a start line 14 and a stop line 15 to the measuring device 8, which it can use to initiate measurement of the actual frequency response and to receive a report of the ascertained measure of the actual frequency response.

[025] As the measure of the frequency response of the filter 1, a time constant is ascertained. To this end, the control device 9 sends a signal via the start line 14 to the measuring device 8, which then starts the measurement by applying a step signal to the input of the filter 1. At the same time, the control device 9 starts a counter which counts upwards in time with the frequency applied via the line 13.

[026] In the meantime, the measuring device 8 monitors the output of the filter 1 for arrival at a particular voltage value. As soon as this value is reached, the measuring device 8 uses the stop line 15 to send a signal to the control device 9, which then stops the counter and normalizes the count reached to the frequency of the applied clock signal. This normalized count then corresponds to a time constant which is supplied to the memory arrangement 10 via a line.

[027] At the same time, the memory arrangement 10 is notified via an input line 11 about which nominal cut-off frequency is to be set. The information which is on the memory arrangement 10 about the nominal cut-off frequency which is to be set and the normalized

time constant are logically combined in the memory arrangement 10 to form a multidigit address signal for a table memory. This table memory stores, for every combination of each adjustable nominal filter frequency and for the possible values of the ascertained digital time constant, an adjustment parameter for adjusting the capacitors 3. If the intention is to be able to set six different filter frequencies, for example, and if the digital value of the normalized time constant is in a range from 0 to 999, then 6000 different adjustment parameters are stored in the memory arrangement 10. The memory arrangement is therefore used as a look-up table for the adjustment parameters.

[028] In this case, the involvement for logically combining the ascertained time constant and for the information about the nominal cut-off frequency for selecting the adjustment parameter, can be simplified by transmitting the information about the nominal filter frequency and about the ascertained time constant, in each case in the form of a binary digital value, to the control device 10 and connecting it there to various lines in an address input which is several bits wide. In this way, no complex logic is required and an ordinary read-only memory can be used for the memory device 10. Since such memories are generally available only with a particular number of memory cells, memory cells are sometimes unused if the number of combinations comprising the number of nominal filter frequencies and the possible time constants is smaller than the number of memory cells.

[029] In addition, however, it is also possible to store the adjustment parameters using a different table memory which is used, for example, as a program store for a microcontroller or processor. This table memory can store the adjustment parameters in an unused memory area,

starting at a particular start address. The address value obtained from the combination of the time constant and the information about the nominal filter frequency would, in such a case, be interpreted as an offset which is added to the start address. This option is particularly appropriate in cases in which the inventive circuit arrangement is integrated in a semiconductor which contains a program-controlled control mechanism with a table memory anyway.

[030] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.